REMARKS

Claims 1-6, 12 and 15-16 have been rejected under 35 U.S.C. 102 as being anticipated by Lu et al. (U.S. Patent 5,963,808).

Claim 1 recites "thermally oxidizing the upper surface of the semiconductor substrate, thereby forming a bottom oxide layer over the upper surface of the semiconductor substrate and simultaneously forming bit line oxide regions over each of the one or more diffusion bit line regions".

The Examiner indicates that Lu et al. teach this step in Fig. 10A, wherein thermal oxide regions 1000a, 1000b and 1000c are formed over diffusion bit line 212, 214 and 216. However, even if the thermal oxide regions 1000a, 1000b and 1000c of Lu et al. correspond with "bit line oxide regions" as recited by Claim 1, the Examiner fails to indicate where Lu et al. teach the simultaneous formation of a "bottom oxide layer" as recited by Claim 1.

For this reason, Claim 1 is not anticipated by Lu et al. Claims 2-6, 12 and 15-16, which depend from Claim 1, are not anticipated by Lu et al. for at least the same reasons as Claim 1.

Claim 1 further recites "and then forming an intermediate dielectric layer over the bottom oxide layer and the bit line oxide regions". (Emphasis added.) The Examiner indicates that elements 1102, 800a-b, 802a-b and 700Aa-Ab, which are illustrated in Fig. 11A of Lu et al., correspond with "an intermediate dielectric layer" as recited by Claim 1. However, Lu et al. teach that elements 800a-b, 802a-b and 700Aa-Ab are fabricated before the thermal oxide regions 1000a, 1000b and 1000c. (See, Lu et al., Fig. 9A.) Thus, the fabrication of elements 800a-b, 802a-b and 700Aa-Ab of Lu et al. do not follow the order

specified by the "and then" clause of Applicants' Claim 1. For this reason, elements 800a-b, 802a-b and 700Aa-Ab of Lu et al. can not correspond with "an intermediate dielectric layer" as recited by Claim 1. The following arguments therefore assume that only the interpoly dielectric 1102 of Lu et al. may correspond with "an intermediate dielectric layer" as recited by Claim 1.

Claim 15 recites "removing the top dielectric layer and intermediate dielectric layer located between the plurality of word lines". As described above, only the interpoly dielectric 1102 of Lu et al. may correspond with the "intermediate dielectric layer" as recited by Claim 15. Lu et al. do not explicitly teach removing the interpoly dielectric 1102 between the word lines. However, the Examiner indicates that the above-recited step of Claim 15 is an "inherent" step of Lu et al., as "the removal is necessary to allow the word line to contact the underlying gates below - this is necessary for the device to be operative". Contrary to the Examiner's assertion, allowing the word line 208 to contact the underlying gates (e.g., floating gate strips 408a and 408b, floating gate coupling caps 1100a and 1100b) would render the memory cell of Lu et al. non-operative. That is, the floating gate elements 408a-408b/1100a-1100b would not store program/erase charge in the desired manner if these floating gate elements were contacted by the word line 208. Lu et al. explicitly teach that the "interpoly dielectric 1102, e.g., oxide-nitrite-oxide (ONO) covers the floating gate coupling caps and insulates them from the polysilicon layer" (i.e., word line 208). (Lu et al. Col. 9, lines 14-16.) Because Lu et al. teach that the purpose of interpoly dielectric layer 1102 is to insulate the floating gate elements from the word line

208, Lu et al. fail to teach or suggest the removal of this interpoly dielectric layer 1102 to allow contact between the floating gate elements and the word line 208 as suggested by the Examiner. For this additional reason, Claim 15 is not anticipated by Lu et al.

Claim 16 recites "wherein the intermediate dielectric layer is formed directly on the bottom oxide layer and the bit line oxide regions". As described above, only the interpoly dielectric 1102 of Lu et al. may correspond with the "intermediate dielectric layer" as recited by Claim 16. Fig. 11A of Lu et al. indicates that the interpoly dielectric 1102 may be formed directly on a portion of thermal oxide region 1000b. However, Lu et al. fail to teach that the interpoly dielectric 1102 is formed directly on any other oxide region that is formed at the same time as thermal oxide region 1000b. Thus, Lu et al. fail to teach that the interpoly dielectric 1102 is also formed directly on any element that may correspond with a 'bottom oxide layer'. For this additional reason, Claim 16 is not anticipated by Lu et al.

Claims 13 and 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al.

Claims 13-14, which depend from Claim 1, are allowable over Lu et al. for at least the same reasons as Claim 1.

CONCLUSION

Claims 1-16 are pending in the present Application. Claims 7-11 are allowable. Reconsideration and allowance of Claims 1-6 and 12-16 is respectfully requested. If there are any questions, please telephone the undersigned at (925) 895-3545 to expedite prosecution of this case.

Respectfully submitted,

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